

What is claimed is:

1. An information processing apparatus comprising:
 - data storing means;
 - first and second data input/output means for giving access to the data storing means;
 - clock generating means for supplying a clock to the second data input/output means;
 - switching means for switching access of the first data input/output means and the second data input/output means to the data storing means; and
 - access arranging means for causing the clock for the second data input/output means to wait and executing the access of the first data input/output means earlier when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated, and for starting the access of the second data input/output means after the access of the first data input/output means is ended.
2. An information processing apparatus comprising:
 - a built-in memory;
 - a processor for processing data stored in the built-in memory;
 - clock generating means for supplying a clock signal to the processor;
 - input/output control means for executing access to the built-in memory upon receipt of an instruction from an external

control device; and

access arranging means for generating a wait request signal to cause the clock signal to wait and carrying out access of the input/output control means with a priority when a contention of access of the processor and the input/output control means to the built-in memory is generated.

3. The information processing apparatus according to claim 2, further comprising selecting means for switching the access of the processor and the input/output control means to the built-in memory,

wherein the access arranging means outputs a control signal to the selecting means when a request for the access of the input/output control means to the built-in memory is generated during the access of the processor to the built-in memory, and

the selecting means receiving the control signal switches the access of the processor to the access of the input/output control means to the built-in memory.

4. The information processing apparatus according to claim 2, further comprising holding means for holding read data output from the built-in memory before a wait operation of the processor during the wait operation of the processor,

wherein the access arranging means switches read data to be supplied to the processor between the read data output from the built-in memory and the read data held by the holding means.

5. A memory access arranging method of an information processing apparatus including data storing means and first and second data input/output means for giving access to the data storing means, comprising the steps of:

causing a clock for the second data input/output means to wait when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated;

executing the access of the first data input/output means earlier; and

canceling the clock wait of the second data input/output means after ending the access of the first data input/output means, and executing the access of the second data input/output means.

6. A memory access arranging method of an information processing apparatus including a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, and input/output control means for executing access to the memory with a higher priority than the processor, comprising the steps of:

generating a wait request signal for causing a clock supplied to the processor to wait when a contention of access of the processor and the input/output control means to the memory is generated;

switching the access of the processor to the access of the input/output control means to the memory; and

canceling the clock wait of the processor after ending the access of the input/output control means to the memory, and executing the access of the processor to the memory.

7. A memory access arranging method of an information processing apparatus having a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, input/output control means for executing access to the memory with a higher priority than the processor, and holding means for holding read data output from the memory before a wait operation of the processor during the wait operation of the processor, comprising the steps of:

holding the read data output from the memory before the wait operation of the processor when a contention of read access of the input/output control means is generated for a period in which the processor gives continuous read access to the memory;

causing a clock supplied to the processor to wait;

executing the access of the input/output control means to the memory; and

canceling the clock wait of the processor after ending the access of the input/output control means to the memory, supplying the data held in the holding means to the processor, and restarting the access of the processor to the memory.